REMARKS

This paper is filed in response to the final official action dated January 10, 2006 ("the official action"). This paper is timely-filed.

Claims 1-3 and 5-9 are pending in this application.

Claims 1-3 and 5-9 currently stand rejected under 35 U.S.C. §103(a) as obvious over admitted prior art in view of U.S. Patent No. 6,410,446 to Tsai *et al.* or over admitted prior art in view of U.S. Patent No. 6,365,015 to Shan *et al.*

By the foregoing, claims 1, 3, 6, 8, and 9 have been amended, and new claims 11 and 12 have been added. Thus, claims 1-3, 5-9, 11, and 12 are presently at issue.

Support for the amendments to claims 1 and 6 may generally be found throughout the application as filed. More specifically, support may be found at page 12, lines 1-8 of the present application. The amendments to claims 3, 8, and 9 merely address matters of form. Support for new claims 11 and 12 may be found in originally-filed claims 4 and 10.

The accompanying amendments are proper under 37 C.F.R. §1.116 practice and should be entered because the rejections set forth in the previous office action have been overcome. Moreover, the amendments should be entered because they place the application in condition for allowance (or in better condition for appeal).

The various bases for the claim rejections are addressed below in the order presented in the official action. Reconsideration of the application, in view of the foregoing amendments and the following remarks, is solicited.

CLAIM REJECTIONS – 35 U.S.C. §103(a)

Claims 1-3 and 5-9 have been rejected under 35 U.S.C. §103(a) as obvious over admitted prior art in view of U.S. Patent No. 6,410,446 to Tsai *et al.* or over admitted prior art in view of U.S. Patent No. 6,365,015 to Shan *et al.*

The Applicant respectfully traverses the rejections as applied to claims 1-3, 5-9, 11, and 12, as presented herein.

A. Independent Claim 1 and Dependent Claims 2, 3, 5, and 11

Claim 1 recites a method of manufacturing a semiconductor device, comprising the steps of providing a semiconductor substrate in which a gate electrode

pattern is formed and forming an interlayer insulating film including a multi-layered oxide film by performing multiple simultaneous deposition-and-etch processes in order to bury the gate electrode pattern, wherein a deposition-and-etch rate of a subsequent deposition-and-etch process is decreased relative to a preceding deposition-and-etch process.

Tsai *et al.* does not disclose or even suggest forming an interlayer insulating film including a multi-layered oxide film by performing multiple simultaneous deposition-and-etch processes in order to *bury the gate electrode pattern*. Tsai *et al.* discloses a method of filling gaps between conductive structures comprising depositing a first dielectric material 204 between the gaps until a thickness of the dielectric material 204 is about 1/3-1/2 of a thickness of the height of the gaps, and then depositing a second dielectric material 206a, 206b on the first dielectric material 204 (204a after sputtering step) until well filling the gaps between the conductive structures 202. *See* Tsai *et al.* at column 4, lines 7-20. In contrast, claims 1-3, 5, and 11 recite performing multiple simultaneous deposition-and-etch processes in order to bury the gate electrode pattern.

Additionally, Tsai *et al.* does not teach or suggest performing multiple simultaneous deposition-and-etch processes in order to bury the gate electrode pattern wherein a deposition-and-etch rate of a subsequent deposition-and-etch process is decreased relative to a preceding deposition-and-etch process. Such a method increases the smoothness of the interlayer insulating film, thereby obviating the need for a subsequent CMP process, as disclosed at page 12, lines 1-8 of the present application.

Shan *et al.* discloses a method of forming an oxide layer over metal lines wherein the deposition-and-etch rate (DSR or D/S) is increased when filling the gaps between the metal lines. *See* Shan *et al.* at column 4, lines 8-9. In contrast, pending claims 1-3, 5, and 11 recite performing multiple simultaneous deposition-and-etch processes in order to bury the gate electrode pattern, wherein a deposition-and-etch rate of a subsequent deposition-and-etch process is decreased relative to a preceding deposition-and-etch process. The Applicant found that better smoothness is obtained by using such a method, and that it is therefore not necessary to carry out a subsequent CMP process.

In view of the foregoing remarks, the Applicant submits that a *prima facie* case of obviousness has not been established, and the rejections of claims 1-3, 5, and 11 as assertedly obvious over admitted prior art in view of Tsai *et al.* or Shan *et al.* should therefore be withdrawn.

B. Independent Claim 6 and Dependent Claims 7-9 and 12

Claim 6 recites a method of manufacturing a semiconductor device, comprising the steps of providing a semiconductor substrate in which a gate electrode pattern is formed, forming a first HDP oxide film over the entire structure by performing a first deposition-and-etch process simultaneously, and forming a second HDP oxide film over the entire structure by performing a second deposition-and-etch process simultaneously, wherein a deposition-and-etch rate of the first deposition and etch process is higher than a deposition-and-etch rate of the second deposition and etch process.

As generally discussed above, Tsai *et al.* does not teach or even suggest a method of manufacturing a semiconductor device comprising forming first and second HDP oxide films *over the entire structure*. Furthermore, also as generally discussed above, Tsai *et al.* does not teach or suggest forming a first HDP oxide film over the entire structure by performing a first deposition-and-etch process simultaneously, and forming a second HDP oxide film over the entire structure by performing a second deposition-and-etch process simultaneously, wherein a deposition-and-etch rate of the first deposition and etch process is higher than a deposition-and-etch rate of the second deposition and etch process. As previously mentioned, such a method increases the smoothness of the interlayer insulating film, thereby obviating the need for a subsequent CMP process, as disclosed at page 12, lines 1-8 of the present application.

Also, as generally discussed above, Shan *et al.* discloses a method of forming an oxide layer over metal lines wherein the deposition-and-etch rate (DSR or D/S) is increased when filling the gaps between the metal lines. *See* Shan *et al.* at column 4, lines 8-9. In contrast, pending claims recite a method of manufacturing a semiconductor device comprising forming a first HDP oxide film over the entire structure by performing a first deposition-and-etch process simultaneously; and forming a second HDP oxide film over the entire structure by performing a second

deposition-and-etch process simultaneously, wherein a deposition-and-etch rate of the first deposition and etch process is higher than a deposition-and-etch rate of the second deposition and etch process. The Applicant found that better smoothness is obtained by using such a method, and that it is therefore not necessary to carry out a subsequent CMP process.

In view of the foregoing remarks, the Applicant submits that a *prima facie* case of obviousness has not been established, and the rejections of claims 6-9 and 12 as assertedly obvious over admitted prior art in view of Tsai *et al.* or Shan *et al.* should therefore be withdrawn.

CONCLUSION

It is submitted that the application is in condition for allowance. Should the examiner wish to discuss any matter of form or procedure in an effort to advance this application to allowance, he is respectfully invited to telephone the undersigned attorney at the indicated telephone number.

Respectfully submitted,

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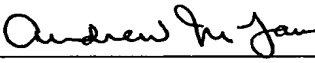

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